Insert 45.2.3.45a, 45.2.3.45b and 45.2.3.45c before 45.2.3.46 for group BIP error counters:

45.2.3.451 Multi-lane BIP mismatch status register (Register 1.300)

The assignment of bits in the multi-lane BIP mismatch status register is shown in Table 45–1391. If the multi-lane PCS described in Clause 82 implements the optional multi-lane BIP mismatch handling (82.2.14.3), this register reflects the values of the hi_bip_mismatch_count and group_bip_mismatch_count variables.

Table 45–139b— Multi-lane mismatch counter, 1 lane register bit definitions

Bit(s)	Name	Description	R/W[a]
3.300.15:6	Reserved	Value always zero, writes ignored	RO
3.300.5	High BIP mismatch count	1 = more than two markers with mismatched BIP in the last alignment marker group 0 = up to two markers with mismatched BIP in the last alignment marker group	RO/LH
3.300.4:0	Multi-lane BIP mismatch count	The number of markers with mismatched BIP in the last alignment marker group	RO

[a]RO = Read only, LH Latching high

45.2.3.45b Multi-lane BIP mismatch counter, 1 lane (Register 1.301)

The assignment of bits in the multi-lane BIP single mismatch counter is shown in Table 45–139b. If the multi-lane PCS described in Clause 82 implements the optional multi-lane BIP mismatch handling (82.2.14.3), this register reflects the value of the group_bip_mismatch_counter<1> variable. When this register is read, the group_bip_mismatch_counter<1> variable shall be set to zero.

Table 45–139b— Multi-lane mismatch counter, 1 lane register bit definitions

Bit(s)	Name	Description	R/W[a]
3.301.15:0	Multi-lane mismatch counter, 1 lane	Cumulative number of 1-lane BIP mismatch in an alignment marker group	RO/NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.45c Multi-lane BIP mismatch counters, 2 through 5 lanes (Registers 1.302 through 1.305)

The behavior of the multi-lane BIP mismatch counters, 2 through 5 lanes is identical to that described for 1 lane in 45.2.3.45b. Multi-lane mismatches of each number of lanes are counted and shown in register bits 15:0 in the corresponding register. Mismatches of 2, 3, and 4 lanes are shown in registers 3.302, 3.303 and 3.304, respectively; Mismatches of 5 or more lanes are shown in register 3.305.

Change 82.2.14 as follows:

82.2.14 Alignment marker ~~removal~~ handling

82.2.14.1 Lane multiplexing and marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes ~~are~~ shall be multiplexed together in the proper order to reconstruct the original stream of blocks. ~~and the~~ The alignment markers ~~are~~ form groups of adjacent blocks on this stream. These alignment marker groups shall be deleted from the data stream. The difference in rate from the deleted alignment markers is compensated for by inserting idle control characters by a function in the Receive process. Note that ~~an~~ alignment marker groups appear in regular

intervals at known locations and are ~~is always~~ deleted ~~when a given PCS Lane is in am_lock=true~~ even if ~~it does~~ individual alignment markers do not match the expected alignment marker value (due to ~~a~~ possible bit error~~s for example~~). Repeated alignment marker errors will result in am_lock being set to false for a given PCS Lane and the deskew process being initiated, but until that happens it is sufficient to ~~delete the block in~~ assume that the alignment marker group appears at its expected position.

82.2.14.2 BIP check

~~As part of the alignment marker removal process~~When a group of alignment markers is removed, the BIP_3 field value of each marker is compared to the calculated BIP value for ~~each~~ the corresponding PCS lane. The result of this comparison is reflected in the am_bip_mismatch<x> variables.

The cumulative number of BIP mismatches in each lane is stored in the bip_error_counter<x> counters. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.200 through 3.219) ~~is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field~~ reflects the value of each of the bip_error_counter counters. If a Clause 45 MDIO is not implemented, then a vendor-specific equivalent implementation of the counters shall be provided instead.

The BIP block error rate on lane *i* can be estimated by the dividing the read value of bip_error_counter<*i*> by the elapsed time since its previous reading The incoming bit error ~~ratio~~ rate can be estimated by dividing the BIP block error ~~ratio~~ rate by a factor of 1081344.

82.2.14.3 Multi-lane BIP mismatch handling

Multi-lane BIP mismatch handling is required for a 100GBASE-R PCS when the optional CAUI-4 physical instantiation is implemented. It is optional for 100GBASE-R PCS without CAUI-4, and for 40GBASE-R PCS.

If implemented, multi-lane BIP mismatch handling shall be as described in this subclause (82.2.14.3).

The purpose of multi-lane BIP mismatch counting is to provide an assessment of the rates of correlated errors events in a multi-lane link. These rates can be used to estimate the mean time to false packet acceptance (MTTFPA).

When a group of alignment markers is removed, the number of markers with mismatched BIP in an alignment marker group (the sum of am_bip_mismatch<x>) is calculated and stored in the group_bip_mismatch_count variable. If group_bip_mismatch_count is greater than two, The variable hi_bip_mismatch_count is set to true, otherwise it is set to false. group_bip_mismatch_count and hi_bip_mismatch_count retain their values between alignment marker groups.

If group_bip_mismatch_count equals *i*, where *i* is between 1 and 5, the counter group_bip_mismatch_counter<*i*> is incremented by 1. If group_bip_mismatch_count is larger than 5, group_bip_mismatch_counter<5> is incremented by 1. Any such increment is performed only once per alignment marker group, so that the group_bip_mismatch_counter<*i*> counters store the cumulative numbers of multi-lane BIP mismatch events.

If a Clause 45 MDIO is implemented, then the Multi-lane BIP mismatch counter registers (registers 3.300 through 3.304) reflect the values of each of the group_bip_mismatch_counter counters. If a Clause 45 MDIO is not implemented, then a vendor-specific equivalent implementation of the counters shall be provided instead.

Change 82.2.16 as follows:

82.2.16 Receive process

The receive process decodes blocks to produce RXD<63:0> and RXC<7:0> for transmission to the XLGMII/CGMII. One XLGMII/CGMII data transfer is decoded from each block. The receive process ~~must~~ shall insert idle control characters to compensate for the removal of alignment markers. If the PCS receive process spans multiple clock domains, it may also perform clock rate compensation via ~~the~~ insertion or deletion of idle or LPI control characters ~~or sequence ordered sets or the insertion of idle control characters~~as specified in 49.2.4.7.

The receive process decodes blocks as specified in the receive state diagram shown in Figure 82–15.

Change the definition for PCS_status in 82.2.18.2.2 to account for group_bip_mismatch_count:

PCS_status

A Boolean variable, ~~that is true~~ If multi-lane BIP mismatch counting is implemented, asserted when align_status is true, hi_bip_mismatch_count is false and hi_ber is false. If multi-lane BIP mismatch counting not is implemented, asserted when align_status is true and hi_ber is false.

Insert the following new variables at appropriate places in 82.2.18.2.2:

am_bip_mismatch<x>

Boolean variable that is asserted during BIP check if lane x alignment marker BIP_3 field value is not equal to the calculated BIP value for PCS lane x, where x = 0:3 for 40GBASE-R and x = 0:19 for 100GBASE-R. It is de-asserted if BIP_3 field value is equal to the calculated BIP value, or if the processed block is not an alignment marker.

group_bip_mismatch_count

If multi-lane BIP mismatch counting is implemented, this variable holds the number of markers with mismatched BIP in the recent alignment marker group.

hi_bip_mismatch_count

If multi-lane BIP mismatch counting is implemented, this Boolean variable is assigned when an alignment marker group is checked. Asserted if group_bip_mismatch_count is larger than two, and de-asserted otherwise. This variable retains its value between alignment marker groups.

Insert the following new counters at appropriate places in 82.2.18.2.4:

bip_error_counter<x>

16-bit counters which hold the accumulated number of am_bip_mismatch<x>, where x = 0:3 for 40GBASE-R and x = 0:19 for 100GBASE-R. These counters are reflected in MDIO registers 3.200 through 3.219. They are cleared on reading and saturated on overflow.

group_bip_mismatch_counter<x>

If multi-lane BIP mismatch counting is implemented, these 16-bit counters count the number of group BIP errors of various lengths. group_bip_mismatch_counter<i> is incremented by one when an alignment marker group with exactly i mismatched BIP fields is encountered, where x = 1:4 for 40GBASE-R and x = 1:5 for 100GBASE-R. These counters are reflected in MDIO registers 3.300 through 3.304. They are cleared on reading and saturated on overflow.

Add the appropriate items to 82.7 PICS.